CLAIMS

What is claimed is:

1. An integrated testing method capable of performing a test procedure concurrently in a multitasking manner on a number of computer components through software simulation, the integrated testing method comprising the steps of:

specifying a total number of simulated operations for testing the components;

specifying a FIFO buffer size for the components;

generating a command sequence including a number of commands based on a first specified random number range, with each command being used to simulate a certain task;

generating a start time of operation based on a second specified random number range;

concurrently activating all the components under test to operate in response to each command from the command sequence; and

in the event that at least two of the components under test are competing for access to a certain resource, activating an arbiter to perform arbitration for these competing components.

2. The integrated testing method of claim 1, wherein the resource is a PCI bus.

3. The integrated testing method of claim 1, wherein the resource is a memory unit.

4. The integrated testing method of claim 1, wherein the components under test include a DMA component, a SIO component, an ISA component, an AC component, an USB component, an IDE component, an AGP component, a PCI component, and a CPU.

5. The integrated testing method of claim 1, wherein the arbiter is a South Bridge chipset.

6. The integrated testing method of claim 1, wherein the arbiter is a North Bridge chipset.

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